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EXAMINER

PROCTOR, JASON SCOTT

ART UNIT

PAPER NUMBER

2123

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/014,831	Applicant(s) ZAMMIT ET AL.	
	Examiner Jason Proctor	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 11-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 11-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 1-19 were rejected in office action dated 25 April 2005. Applicants' response has amended claims 1, 7, 11, 12, 16, 18, and 19 and canceled claim 10. Claims 1-9 and 11-19 have been submitted for reconsideration.

Priority

1. The Examiner acknowledges Applicants' request for priority to Great Britain application 0030735.5 filed on December 15, 2000. Receipt is acknowledged of papers submitted under 35 U.S.C. § 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 10-12 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. At issue were method steps that decide a problem known in computer science as the Halting Problem, which is proven to be unsolvable. The Examiner referred to "Introduction to the Theory of Computation", by Michael Sipser, ©1997, particularly section 5.1, to teach what is known in the art concerning the Halting Problem.

In response, Applicants argue primarily that (emphasis in original):

Amended claim 1 recites the step of *analyzing the loop termination condition to determine whether it is possibly non-terminating*. Claim 1 does not recite that the loop is analyzed for definite non-termination. Certainly it is possible to analyze a loop termination condition to determine if it may be non-terminating.

“Possibly non-terminating”, as recited in claim 1, is substantially different from definitely non-terminating, as would be required to solve the “Halting Problem”. Thus, claim 1 does not recite steps that decide a problem known as the Halting Problem. While the Examiner refers to page 50, lines 13-14 as describing a method that would include solving the Halting Problem, this is irrelevant in the present instance. As noted above, claim 1 uses the word “possibly”. Whether or not the specification discloses a method that could be interpreted as solving the halting problem is not at issue. The issue is what is actually claimed. With respect to claim 1, it does not recite a method that could include solving the halting problem.

The Examiner has considered Applicants’ argument and has found it persuasive. Indeed, it is possible to analyze a loop termination condition to determine if it may be non-terminating. The previous rejections under 35 U.S.C. § 112, first paragraph, for failing to comply with the enablement requirement have been withdrawn. However, Applicants’ arguments have illustrated that the written description of the application fails to disclose critical details of determining and defining “possibly non-terminating loop conditions”.

3. Claims 1-9 and 11-19 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Independent claims 1, 16, 18, and 19 recite the limitation “analyzing the loop termination condition to determine whether it is possibly non-terminating” which is not described in the specification.

Applicants’ arguments shown above highlight that the specification fails to disclose what is meant by “possibly non-terminating” and how Applicants’ invention determines whether a loop is possibly non-terminating. In particular, page 50, lines 1-14 of the specification state:

[The sequential code generator:]

(2) Analyses the loop to check whether it is possibly non-terminating, or whether it definitely terminates. Methods for checking whether a loop definitely terminates include:

(a) checking whether the loop represents a standard for loop (that is, a counter is set to an initial value, the terminating condition checks whether the counter has reached a max/minvalue, and the counter IB Increased/decreased monotonically at each execution of the loop body).

(b) checking whether every execution of the S-body reaches an exit point.

Applicants' arguments above regarding these teachings are persuasive. The claim uses the term "possibly". The previous interpretation of the claim limitations were such that a "non-terminating loop" is at least a "possibly non-terminating loop" and therefore written description was found at page 50, lines 1-14. However, Applicants have argued that this portion of the specification is not what is claimed:

While the Examiner refers to page 50, lines 13-14 as describing a method that would include solving the Halting Problem, this is irrelevant in the present instance. As noted above, claim 1 uses the word "possibly". Whether or not the specification discloses a method that could be interpreted as solving the halting problem is not at issue. The issue is what is actually claimed. With respect to claim 1, it does not recite a method that could include solving the halting problem.

Subsequently, the specification discloses methods (a) and (b) for determining whether a loop definitely terminates. The specification fails to define what a "possibly non-terminating loop" is or methods for determining if a particular loop is "possibly non-terminating". It is noted that FIG. 25 shows the code generation of loops that may not terminate, however FIG. 25 discloses neither the definition of a "possible non-terminating loop" nor how to detect such a loop.

For example, there is no description in the application which would convey to one skilled in the relevant art how the claimed invention performs when confronted with the following loop:

```
while (n != 1) {  
    If (n is odd) { n = 3 * n + 1 } else { n = n / 2 }  
}
```

It is clear that under certain circumstances, this loop definitely terminates. This particular loop is the subject of considerable scientific study and is generally believed to terminate for all positive

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integer values of n , however no proof is known. Does Applicants' invention define this as a "possibly non-terminating loop," in recognition that a person of ordinary skill in the art of computer science must acknowledge that there is no proof that the loop terminates for all inputs? What is the claimed invention's method of "analyzing the loop termination condition"? This method is not described by the specification.

Another example would be the following loop:

```
for (int i = 0; i < 2; i++) {  
    i = 0  
}
```

This loop conforms precisely to Applicants' disclosed method of determining that a loop definitely terminates (page 50, lines 6-11) however it would be trivial for a person of ordinary skill in the art to identify that this is an infinite loop. Does Applicants' invention, by some undisclosed process, somehow identify that this loop is at least "possibly non-terminating"?

For completeness, a third example would be the following loop:

```
for (int i = 0; i < 2; i++) {  
    i = i  
}
```

This loop definitely terminates. However, the method by which Applicants' invention distinguishes this loop from the previous two examples, or any other loop, is entirely undisclosed.

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The specification does not describe how the invention “analyzes the loop termination condition to determine whether it is possibly non-terminating”. The specification does not describe what is meant by a “possibly non-terminating loop”. It is unclear if any of the above examples constitute a “possibly non-terminating loop” in the context of the claims.

As in the previous office action, the Examiner respectfully suggests amended claim language that clarifies what is meant by “analyzing the loop termination condition” and what is meant by “possibly non-terminating”. No new matter may be added.

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Applicants’ arguments regarding the previous rejections of claims 1, 10-12, 16, 18, and 19 have been fully considered and found persuasive. Those rejections have been withdrawn.

4. Claims 11 and 12 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 11 and 12 are heavily amended and appear to recite, in clean form, the following:

A method as claimed in claim 8 [9], in which the converting step (b) comprises:

the scheduler placing at the exit point the at least one discrete process in the list of active unhandled processes with a new entry point.

The meaning of this limitation is unknown. It is unclear if the word "placing" should be "replacing". These claims depend from claim 8, which recites "a list of active unhandled processes having respective exit points". None of the dependent claims appear to remove the processes from that list, therefore it seems that "placing the at least one discrete process [into] the list of active unhandled processes" is an incorrect interpretation of this limitation because the processes are already present in the list. The interpretation that the scheduler places at least one discrete process (found in the list of active unhandled processes) at the exit point is not understood and fails to account for the phrase "with a new entry point". It is unclear how to properly interpret this limitation. Clarification is required.

Claim Rejections - 35 USC § 101

35 U.S.C. § 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1-9 and 11-15 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Regarding claim 1, MPEP 2106 (II) (A) reads as follows:

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." *State Street*, 149 F.3d at 1373, 47 USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (*Brenner v. Manson*, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96); *In re Ziegler*, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)). Accordingly, a complete disclosure should contain some indication of the practical application for the claimed invention, i.e., why the applicant believes the claimed invention is useful.

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Claim 1 recites “a method of co-simulating” which does not produce a useful, concrete, and tangible result. The recited steps include “providing at least one first model”, “converting the at least one first model”, “providing at least one second model”, and concludes with “applying the at least one software model in the at least one first language and the at least one second model in the at least one second language to the simulation engine”. As indicated above, the proper interpretation of the concluding step of claim 1 is unknown, however it appears that the broadest reasonable interpretation is not limited to production of a useful, concrete, and tangible result as required by MPEP 2106 (II) (A).

In response, Applicants’ argue primarily that:

MPEP §2106 II(A) does not require that the claim explicitly recite a “result”. Instead, the claimed invention as a whole must provide a useful, concrete and tangible result. Claim 1 of the present application satisfies the requirements of §101. For example, the method of claim 1 provides a co-simulation method, and recites specific steps for the co-simulation method. The result of the method provides faster co-simulation than prior art methods of co-simulation (see, e.g., page 15 of the specification). Further, claim 1 recites features that make the above results possible, and such features are not “nonfunctional descriptive material”, as discussed in §101. Additionally, co-simulation itself is advantageous in that it enables one to verify a design prior to actual hardware implementation of the design, thereby saving fabrication time and expense.

The Examiner respectfully traverses this argument as follows:

The Examiner presumes that Applicants’ reference to “nonfunctional descriptive material, as discussed in §101” should correctly refer to MPEP 2106.

The Examiner thanks Applicants for their analysis of MPEP 2106. However, the Examiner maintains that the recited method of claim fails to produce a useful, concrete, and tangible result. Applicants’ arguments that co-simulation is useful are persuasive, however utility is insufficient to establish a statutory process [*“However, the mere fact that the claim may satisfy the utility requirement of 35 U.S.C. 101 does not mean that a useful result is achieved*

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under the practical application requirement.” MPEP 2106(II)(A)]. Applicants have not established what the useful, concrete, and tangible result of the method might be.

Applicants’ have submitted that “Figs. 9 and 10 illustrate several models being applied to the simulation engine, which then produces a simulation result”. While Figs. 9 and 10 may illustrate this, the Examiner emphasizes that the claim does not recite or require producing a simulation result. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. The unconventional choice of language, “applying [models] to a simulation engine”, makes it difficult to ascertain whether the limitation requires performing a simulation.

Therefore the Examiner maintains the original analysis that, as written, claim 1 fails to produce a useful, concrete, and tangible result. Therefore, although co-simulation may useful indeed, the claim defines a nonstatutory method and is rejected under 35 U.S.C. § 101.

Regarding the previous rejection of claims 18 and 19 under 35 U.S.C. § 101, Applicants’ amendments to the claims have overcome these rejections. Those rejections have been withdrawn.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Interpretation

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In the interest of compact prosecution, the Examiner makes the following claim interpretations in order to apply prior art to the claims. See *Ex parte Ionescu*, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984).

Claim 1 has been interpreted where “applying to the simulation engine” means “providing as input and performing the simulation”.

Claim 13 appears to recite additional steps of the method of claim 1 that are performed by a human operator. The steps of “checking whether the result of the co-simulation is correct” and “checking whether the digital circuit is synthesizable” appear to be steps of human cognition. It is therefore not unreasonable to interpret the step of “generating a low-level hardware description of the digital circuit” as performed by a human, perhaps by using a computer aided design system of prior art. This reasonable interpretation of claim 13 results in limitations that are entirely performed by a human being.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-7, 13-14, and 16-19 are rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,870,588 to Rompaey et al. (Rompaey).

Regarding claim 1, Rompaey discloses a method of simulating a digital system comprising simultaneous low-level and high-level simulation (column 6, lines 35-44). Rompaey

calls the design environment for this simulation “CoWare” (column 10, lines 53-62). CoWare supports high-level hardware description language models of system components (column 11, lines 45-58; DFL, VHDL) as well as hardware description language models (column 12, lines 45-50). Naturally the high-level programming language models need to be compiled before they can be simulated (column 17, lines 29-58). The CoWare system supports four major design activities, including co-simulation (column 11, lines 12-15). The claimed invention is disclosed with an exemplary embodiment (summarized at column 22, lines 26-35).

Therefore Rompaey anticipates the invention of claim 1 by teaching a co-simulation system where a first portion of the system can be modeled in a high-level programming language as a first model, the first model is converted by compiling the high-level programming language, a second portion of the system can be modeled in a second language, and the overall system is co-simulated by executing both the first model and the second model and simulating their interaction.

To specifically address the amended limitation “wherein converting includes generating, for at least one discrete process, software code including a program loop having a jump instruction and a loop termination condition, and analyzing the loop termination condition to determine whether it is possibly non-terminating, and if so, replacing the jump instruction with an exit point”, the Examiner respectfully submits the following:

This limitation essentially recites two steps: a step of generating a loop, and a step of analyzing a component of that loop. The claim does not recite how the generated loop is in any way related to the surrounding steps or elements recited by the claim. For example, there is no indication of how the generated loop reflects or represents any part of the “one first model” if

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indeed there is any connection between them. Regardless of the difficulties under 35 U.S.C. § 112 presented by this limitation, it appears to recite a sequence of arbitrary steps unrelated to the surrounding method. As a result, these limitations do not further limit the claimed invention. Because these steps are unrelated to the surrounding method, the result of the method would be functionally unchanged were these steps omitted.

Applicants' argue primarily that:

The Examiner, in rejecting original claim 10 under § 103(a), without rejecting claim 10 under § 102, effectively admits that *Rompaey* does not teach or suggest this feature. Moreover, *Rompaey* has not been found to teach or suggest these above features. Since these feature are now included in amended claim 1, *Rompaey* does not anticipate amended claim 1 for at least the same reasons that it does not anticipate original claim 10.

The Examiner respectfully traverses this argument as follows:

The Examiner is unaware of the admission to which Applicants refer. As Applicants have identified elsewhere, claims 10-12 as originally filed were interpreted as implementing preemptive scheduling. Applicants have stated for the record that these limitations "do not pertain to preemptive scheduling". It is unclear to the Examiner how an admission that *Rompaey* may not disclose all aspects of preemptive scheduling known in the art can be being interpreted as an admission that *Rompaey* does not disclose generating and analyzing a loop.

Nevertheless, as explained above, the limitations referred to by Applicants do not further limit the invention. *Rompaey* therefore anticipates the claimed invention. Applicants' arguments have been fully considered, but have been found unpersuasive.

Regarding claim 2, *Rompaey* discloses the converting step comprises compiling the first model (column 12, lines 45-50).

Regarding claim 3, Rompaey discloses that the high-level hardware language is based on a communicating sequential process model (column 11, line 59 – column 12, line 5).

Regarding claim 4, Rompaey discloses that the first part of a digital system is represented as a plurality of concurrent processes that communicate with each other (column 11, line 59 – column 12, line 5; column 12, lines 23-34) and converting the concurrent processes to a sequential software process (column 12, lines 44-49; column 16, lines 6-17; column 16, lines 24-30).

Regarding claim 5, Rompaey discloses a port and protocol hierarchy that distinguishes between the functional and communication behavior (column 16, line 31-65). Included in this are references to a *handshake* (column 16, lines 42-45). A handshake is functionally equivalent to a stimulus and a response.

Regarding claim 6, Rompaey discloses a port and protocol hierarchy that distinguishes between the functional and communication behavior (column 16, line 31-65). It is inherent that components in CoWare respond to the stimulus by performing a desired behavior of at least one part of the digital system. This concept is the premise of Rompaey's invention; violating this premise would render the invention useless.

Regarding claim 7, Rompaey discloses an exemplary embodiment including a sample clock generator (column 21, lines 34-59). Rompaey discloses simulating a plurality of discrete processes (column 6, lines 57-64). As CoWare is a computer-implemented system (column 15, lines 50-62) and, in at least one embodiment, executes concurrent processes on a single processor (column 22, lines 52-59), it is inherent that CoWare uses a scheduler. Failure to use a scheduler, as well known in the art, would diminish the utility of the system such that it would be nearly inoperable.

Regarding claim 13, Rompaey discloses steps of synthesizing the circuit (column 11, lines 12-20) and generating a low-level hardware description of the circuit (column 28, lines 23-30).

Regarding claim 14, Rompaey discloses that the disclosed system is to be used as a method of manufacturing a circuit (column 6, lines 7-18).

Regarding claims 16-19, Rompaey discloses that the disclosed system is embodied on a computer apparatus (column 15, lines 50-62). The CoWare system interfaces with an application programmer's interface (API) (column 15, lines 50-52) therefore it is inherent that the CoWare system is a computer program. It is inherent that the computer program is stored on a computer-readable medium. These claims are rejected for the reasons cited here as well as provided above in the context of claim 1.

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Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 8, 9, 11, and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Rompaey.

Claims 8, 9, 11, and 12 recite limitations regarding a scheduler. Official notice is taken that all of the recited capabilities or functions of the scheduler are well known in the art. While it is inherent that the system of Rompaey uses some form of scheduler, the particular features of that scheduler may not be inherent. However, it would have been obvious to a person of ordinary skill in the art to incorporate well-known capabilities and functions of a scheduler with the scheduler of Rompaey in order to benefit from the well-known properties of those capabilities and features.

8. Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Rompaey in view of "Pentium® Pro Processor Performance Brief" by Intel, © 1997.

Regarding claim 15, Intel shows a well-known integrated circuit (entire document, especially pages 5-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to produce an integrated circuit, such as the Pentium® Pro Processor, using the method disclosed by Rompaey.

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Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

jsp


Paul L. Rodriguez 11/9/05
Primary Examiner
Art Unit 2125